Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An impedance trimming circuit comprising:

a common bias section composed of a first series circuit having a first ~~internal~~ resistor and ~~an external~~ a second resistor connected in series via a first node and a first operational amplifier having a first input terminal ~~connected to an internal~~ being inputted a reference voltage, a second input terminal connected to the first node, ~~and an output terminal connected to the first series circuit~~ wherein an output signal of the first operational amplifier controls a voltage of the first node; and

an impedance trimming section composed of a second series circuit having a ~~second internal~~ third resistor and an impedance dummy resistor connected in series via a second node, a comparator having a first input terminal connected to the first node and a second input terminal connected to the second node, a code control circuit ~~which uses a clock signal to latch~~ latching an output signal from the comparator to generate ~~a plurality of~~ switching codes, ~~and a switching circuit~~ which ~~uses the plurality of switching codes to switch~~ controls a ~~resistance~~ value of the impedance dummy resistor,

wherein the ~~first operational amplifier is also connected to the second series circuit, and an output signal from the code control circuit is inputted to~~ switching codes control a value of a target impedance trimming resistor.

2. (currently amended) The impedance trimming circuit according to claim 1, which further comprises a code flattening section configured to latch one of the plurality of switching codes output from the code control circuit, the code flattening ~~circuit~~ section fixes a ~~resistance~~ value of the target impedance trimming resistor based on said one of the plurality of switching codes.

3. (original) The impedance trimming circuit according to claim 2, wherein when said one of the plurality of switching codes output from the code control circuit repeatedly periodically varies, said one of the plurality of switching codes is latched by the code flattening section.

4. (currently amended) The impedance trimming circuit according to claim 3, wherein values of the plurality of switching codes output from the code control circuit increase by degrees in accordance with an output signal of the comparator, and when ~~the~~ a value of one of the plurality of switching codes decreases at first, the code flattening circuit latches one of the plurality of switching codes.

5. (original) The impedance trimming circuit according to claim 3, wherein each of the plurality of switching codes is expressed by n bits (n = more than 1), and when said one of the plurality of switching codes output from the code control circuit repeatedly periodically varies between two bits, the code flattening circuit latches one of the two bits.

6. (original) The impedance trimming circuit according to claim 3, wherein each of the plurality of switching codes is expressed by n bits (n = more than 1), and when said one of the plurality of switching codes output from the code control circuit repeatedly periodically varies between three bits, the code flattening circuit latches an intermediate one of the three bits.

7. (currently amended) The impedance timing circuit according to claims 1 ~~or 2~~, wherein ~~one or more pairs of~~ the common bias section and the impedance trimming section ~~are present~~ comprise a unit.

8. (currently amended) The impedance timing circuit according to claims 1 ~~or 2~~, wherein the impedance dummy resistor includes an output buffer.

9. (currently amended) The impedance timing circuit according to claims 1 ~~or 2~~, wherein the impedance dummy resistor includes input impedance, terminal resistance, and pull-up resistance or pull-down resistance.

10. (currently amended) The impedance timing circuit according to claims 1 ~~or 2~~, wherein the plurality of switching codes from the switching circuit and a ~~resistance~~ value of the

impedance dummy resistor exhibit a reciprocal relationship, a polygonal-line relationship, or an S shaped relationship.

11. (currently amended) The impedance timing circuit according to claims 1 ~~or 2~~, wherein ~~resistance~~ values ~~for~~ of the first and ~~second internal~~ third resistors contain parasitic resistance parasitic on a package, a lead, or a frame, and are adjusted to shift an adjustment range of ~~the resistance~~ a value of the impedance dummy resistor.

12. (currently amended) The impedance timing circuit according to claims 1 ~~or 2~~, wherein the ~~external~~ second resistor is an ~~external~~ accurate resistor, and ~~the resistance~~ values ~~for~~ of the first and ~~second internal~~ third resistors ~~can be switched on the~~ are decided on the basis of a value [[for]] of the ~~external~~ second resistor.

13. (currently amended) The impedance timing circuit according to claims 1 ~~or 2~~, wherein ~~the resistance~~ values ~~for~~ of the first and ~~second internal~~ third resistors are ~~switched~~ decided on the basis of the parasitic resistance parasitic on [[the]] a package, lead, and frame, as well as the value [[for]] of the ~~external~~ second resistor.

14. (currently amended) The impedance timing circuit according to claims 1 ~~or 2~~, wherein the first ~~internal~~ resistor is composed of a first and second resistance elements, the first resistor generates a voltage equal to a difference between a value [[for]] of the ~~internal~~ reference ~~value~~ voltage during design and a value [[for]] of the ~~internal~~ reference ~~value~~ voltage during operation, and ~~reference~~ values of the first and second resistance elements are adjusted in accordance with [[the]] a value for the ~~internal~~ reference ~~value~~ voltage so as to meet the following relationship:

$$Rext : R1under + R1upper = Rtrim : Rt$$

(where Rext denotes ~~the resistance~~ a value of the ~~external~~ second resistor, R1under denotes ~~the resistance~~ a value of the first resistance element, R1upper denotes ~~the resistance~~ a value of the ~~second~~ resistance element, Rtrim denotes ~~the resistance~~ a value of the impedance dummy resistor, and Rt denotes a ~~resistance~~ value of the ~~second internal~~ third resistor).

15. (currently amended) The impedance timing circuit according to claims 1 ~~or 2~~, wherein the ~~external~~ second resistor is replaced with ~~an internal~~ a resistor which operates more accurately than the first and ~~second internal~~ third resistors and impedance dummy resistor.

16. (currently amended) The impedance timing circuit according to claims 1 ~~or 2~~, wherein the impedance trimming section has a second operational amplifier, a first input terminal of the second operational amplifier is connected to the first series circuit, and a second input terminal and an output terminal of the second operational amplifier are connected to the second series circuit.

17. (currently amended) The impedance trimming circuit according to claims 1 ~~or 2~~, wherein ~~the resistance~~ a value of the impedance dummy resistor maintains a relationship with ~~the resistance~~ a value of the target impedance trimming resistor such that the ~~resistance~~ value of the impedance dummy resistor is an integer number of times greater than the ~~resistance~~ value of the target impedance trimming resistor.

18. (currently amended) The impedance trimming circuit according to claims 1 ~~or 2~~, wherein the impedance trimming section is one of an output impedance trimming section and an input impedance trimming section, the output impedance trimming section being configured to trim an output impedance, the input impedance trimming section being configured to trim an input impedance.

19. (currently amended) An impedance trimming circuit comprising:

a common bias section comprising a first series circuit and a first operational amplifier, the first series circuit including a first ~~internal~~ resistor and ~~an external~~ a second resistor are connected in series via a first node, the first operational amplifier including a first input terminal to which ~~an internal~~ a reference voltage is to be applied, and a second input terminal connected to the first node, ~~and an output terminal connected to the first series circuit~~ wherein an output signal of the first operational amplifier controls a voltage of the first node;

an output impedance trimming section comprising a second series circuit, a first comparator and a first code control circuit, the second series circuit including a third ~~second~~

~~internal~~ resistor and an output impedance dummy resistor which are connected in series via a second node, the first comparator including a first input terminal connected to the first node, and a second input terminal connected to the second node, the first code control circuit latching an output signal [[of]] from the first comparator ~~as a clock signal, and outputting one of a plurality of~~ to generate first switching codes which control a value of the output impedance dummy resistor; and

an input impedance trimming section comprising a third series circuit, a second comparator and a second code control circuit, the third series circuit including a ~~third internal~~ fourth resistor and an input impedance dummy resistor which are connected in series via a third node; the second comparator including a first input terminal connected to the first node and a second input terminal connected to the third node, the second code control circuit latching an output signal [[of]] from the second comparator ~~as the clock signal, and outputting one of a plurality of~~ to generate second switching codes which control a value of the input impedance dummy resistor,

wherein:

~~the output terminal of the first operational amplifier is connected to the second and third series circuits;~~

~~a resistance value of the output impedance dummy resistor and a resistance~~ the first switching codes control a value of a first target impedance trimming resistor, ~~are changed by using one of the plurality of first switching codes, the resistance value of the first target impedance trimming resistor being to be subjected to actual output impedance trimming;~~ and

~~a resistance value of the input impedance dummy register and a resistance~~ the second switching codes control a value of a second target impedance trimming resistor ~~are changed by using one of the plurality of second switching codes, the resistance value of the second target impedance trimming resistor being to be subjected to actual input impedance trimming~~.

Amendments to the Drawings:

Please designate Figures 19-21 by --Prior Art--.

The attached sheets of drawings includes changes to Figures 19-21. These sheets, which include Figures 19-21, replace the original sheets including Figures 19-21.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes